

PEAK POWER AND ENVELOPE MAGNITUDE REGULATORS AND CDMA
TRANSMITTERS FEATURING SUCH REGULATORS

This application is a Continuation-in-Part of co-pending application serial No. 09/200759 entitled "PEAK POWER AND ENVELOPE MAGNITUDE REGULATORS AND CDMA TRANSMITTERS FEATURING SUCH REGULATORS", filed on November 26, 1998 by the inventors of the present application and assigned to the assignee of the present application.

FIELD OF THE INVENTION

This invention relates generally to control of power and more specifically to peak power regulation.

BACKGROUND OF THE INVENTION

The use of Code Division Multiple Access (CDMA) technology is increasing within wireless applications such as cellular and Personal Communication Systems (PCS). Its utilization will continue to be significant as CDMA technology is incorporated within new standards such as the third generation (3G) Direct Spreading (DS) - CDMA communication system currently being defined. In CDMA technologies, multiple users and/or multiple data streams of each user, which each transmit information on a different code channel, share the same frequency channel, hereinafter referred to as a carrier. Furthermore, CDMA transmitters may also utilize multiple carriers, and therefore, multiple CDMA carriers share the same power amplifier and other components within a particular transmitter. This sharing of carriers between users and/or the sharing of power amplifiers and other components between carriers cause compounded signals to have a high Peak to Average Power Ratio (PAPR) to be processed by said components. In the 3G DS-CDMA standards, multiple code channels share the same carrier within 3G

mobile stations. Hence, similar to that for a base station, compounded signals with potentially high PAPR are input to the power amplifiers of 3G mobile stations.

In order to meet the out-of-band emissions requirements, a power amplifier and other components with this high PAPR input is required to provide good linearity in a large dynamic range. This makes the power amplifier one of the most expensive components within the communication system. The high PAPR also means that the power amplifier operation has low power efficiency. When considering the 3G DS-CDMA case, this low power efficiency reduces the battery life time for 3G mobile stations.

An apparatus is thus needed that can reduce the PAPR of CDMA signals input to power amplifiers. Such a device should reduce the peaks of the compounded input signals such that a less expensive power amplifier can be utilized with out-of-band emissions still being fully controlled. This device should also be relatively inexpensive and any degradation in terms of in-band signal quality should be within an acceptable range.

SUMMARY OF THE INVENTION

The present invention is directed to peak power and envelope magnitude regulators that function preferably within a Code Division Multiple Access (CDMA) transmitter. These regulators operate to reduce peak power spikes within input signals, controlling the out-of-band emissions, and maintaining the in-band signal quality within an acceptable degradation.

The present invention, according to a first broad aspect, is a peak power regulator, input with at least one input signal, that outputs at least one output signal

corresponding to the input signal. The power regulator, in this aspect, consists of a first and second delay apparatus, a power estimation apparatus, a scaling factor generator, an excess power correction generator, a filtering apparatus and an excess power removal apparatus. The first and second delay apparatus generate first and second delayed signals corresponding to the input signal. The power estimation apparatus generates, with use of the input signal, an overall input power estimation signal corresponding to the input signal. The scaling factor generator generates a scaling factor with use of the overall input power estimation signal and a maximum acceptable power signal. The excess power correction generator utilizes the scaling factor and the first delayed signal to generate an excess power correction signal. The filtering apparatus filters the excess power correction signal to generate a filtered excess power correction signal. And, the excess power removal apparatus utilizes the filtered excess power correction signal and the second delayed signal to generate the output signal.

20 According to a second broad aspect, the present invention is an envelope magnitude regulator, input with at least one IF input signal, that outputs at least one IF output signal corresponding to the IF input signal. In this aspect, the envelope magnitude regulator includes first and second delay apparatus, an envelope magnitude estimation apparatus, a scaling factor generator, an excess power correction generator, a filtering apparatus and an excess power removal apparatus. The envelope magnitude regulator generates first and second delayed IF signals corresponding to the IF input signal. The envelope magnitude estimation apparatus generates, with use of the IF input signal, an

overall input envelope magnitude estimation signal corresponding to the IF input signal. The scaling factor generator generates a scaling factor with use of the overall input envelope magnitude estimation signal and a maximum acceptable envelope magnitude signal. The excess power correction generator utilizes the scaling factor and the first delayed IF signal to generate an excess power correction signal. The filtering apparatus filters the excess power correction signal to generate a filtered excess power correction signal. And, the excess power removal apparatus that utilizes the filtered excess power correction signal and the second delayed IF signal to generate the IF output signal.

The present invention, according to a third broad aspect, is a method for regulating output power in a peak power regulator, input with at least one input signal, that outputs at least one output signal corresponding to the input signal. In this aspect, the method includes estimating the overall input power level corresponding to the input signal, generating a scaling factor with use of the estimate of the overall input power level and a maximum acceptable input power signal, delaying the input signal by a first amount, generating an excess power correction signal with use of the scaling factor and the input signal delayed by the first amount, filtering the excess power correction signal, delaying the input signal by a second amount larger than the first amount and generating the output signal with use of the input signal delayed by the second amount and the filtered excess power correction signal.

In other aspects, the present invention is a CDMA transmitter incorporating a peak power regulator or envelope

magnitude regulator according to one of the above aspects of the present invention.

Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described with reference 10 to the following figures, in which:

FIGURE 1 is a block diagram of a single carrier transmitter according to an embodiment of the present invention;

FIGURE 2 is a functional block diagram of a first 15 implementation of a single carrier Baseband Peak Power Reduction (PPR) block used in the transmitter of FIGURE 1;

FIGURE 3 is a block diagram of a multi-carrier transmitter according to another embodiment of the present invention;

FIGURE 4a is a functional block diagram of a first 20 implementation of a multi-carrier Baseband PPR block used in the transmitter of FIGURE 3;

FIGURE 4b is an alternative embodiment for the envelope magnitude predictor used in the multi-carrier 25 Baseband PPR block of FIGURE 4a;

FIGURE 5 is a block diagram of a multi-carrier transmitter according to yet another embodiment of the present invention;

FIGURE 6 is a functional block diagram of a first 30 implementation of a multi-carrier Intermediate Frequency (IF) PPR block used in the transmitter of FIGURE 5;

FIGURE 7 is a functional block diagram of a possible envelope detector used in the IF PPR block of FIGURE 6;

5 FIGURE 8a is a functional block diagram of a second implementation of a single carrier Baseband PPR block used in the transmitter of FIGURE 1;

FIGURE 8b is a functional block diagram of a third implementation of a single carrier Baseband PPR block used in the transmitter of FIGURE 1;

10 FIGURE 9 is a functional block diagram of a second implementation of a multi-carrier Baseband PPR block used in the transmitter of FIGURE 3;

15 FIGURE 10 is a functional block diagram of a multi-carrier combiner that could be used with the single carrier Baseband PPR block of FIGURE 2, 8a and 8b to perform the operation of a multi-carrier Baseband PPR block;

FIGURE 11 is a block diagram of a multi-carrier transmitter including the multi-carrier combiner of FIGURE 10; and

20 FIGURE 12 is a functional block diagram of a second implementation of a multi-carrier IF PPR block used in the transmitter of FIGURE 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

25 Embodiments of the present invention are directed to Peak Power Reduction (PPR) blocks that can be implemented within CDMA transmitters. Although the embodiments of the present invention described herein below are incorporated within CDMA transmitters, the present invention is not limited to such an implementation. For example, the PPR blocks according to the present invention can be utilized in any transmitter in which peak power reduction and control of

out-of-band emissions is required.

A single channel CDMA transmitter using a Baseband Peak Power Reduction (PPR) block according to an embodiment of the present invention is now described with reference to FIGURE 1. A Data Source (DS) 102 generates data streams 104 for transmission on multiple code channels corresponding to multiple users and/or multiple data streams for each user. These data streams 104 from the DS 102 are encoded, spread, and combined within a Channel Encoder and Spreader (CES) 106 which outputs an in-phase (I) baseband signal 108 and a quadrature (Q) baseband signal 110. The I and Q baseband signals 108,110 are then pulse shaped by a Baseband Pulse Shaping Filter (BPSF) 112 that outputs pulse shaped I and Q baseband signals 114,116 to a Baseband PPR block 118, implementations of which are described in detail herein below with respect to FIGURES 2, 8a and 8b. The outputs from the Baseband PPR block 118 are peak power reduced baseband signals 120,122 which are subsequently modulated within a Quadrature Modulator (QM) 124. The output signal 126 from the QM 124 is input to an Up-Converter (UC) 128 which shifts the frequency of the signals to the desired transmitting frequency. The up-converted signal 130 output from the UC 128 is input to Power Amplifier (PA) 132. The output signal 134 from the PA 132 is filtered by an RF Filter (RFF) 136 before being transmitted to the air through an antenna 138.

It is well known that the UC 128 may involve multiple stage up-conversion operations. Also, not shown within FIGURE 1 is the conversion of the data information signal from digital to analog format. This conversion is preferably done either between the Baseband PPR block 118 and the QM 124 or anywhere between the QM 124 and the final

up-conversion stage of the UC 128. In other embodiments of the present invention, described in detail herein below with reference to FIGURES 5, 6, and 7, the Baseband PPR block 118 is removed and an Intermediate Frequency (IF) PPR block is
5 included after the QM 124.

FIGURE 2 illustrates a first implementation of the Baseband PPR block 118 implemented within the single carrier transmitter depicted in FIGURE 1. This Baseband PPR block 118 utilizes nonlinear baseband processing to instantaneously
10 scale the pulse shaped I and Q CDMA baseband signals 114,116 to within an acceptable threshold range. The scaling of the baseband signals results in the envelope of modulated CDMA signals being equivalently scaled to a pre-configured magnitude threshold after quadrature modulation.

15 The Baseband PPR block 118, depicted within FIGURE 2, comprises a squared envelope magnitude predictor 202 input with the I and Q baseband signals 114,116, a multiplier 204 input with the output from the squared envelope magnitude predictor 202 and a configurable threshold signal T, a
20 mapping table 206 input with the output from the multiplier 204, a mean power regulator 208 input with the output of the mapping table 206, a delay block 210 input with the I and Q baseband signals 114,116, multipliers 212 input with the outputs from the delay block 210 and the mean power regulator
25 208, and a Lowpass Filter (LPF) block 214 input with the outputs from the multipliers 212, that generates the baseband outputs 120,122 to the Baseband PPR block 118 which are subsequently input to the QM 124. The LPF block 214 comprises two LPFs, one for each of the outputs from the
30 multipliers 212.

The squared envelope magnitude predictor 202, which

is equivalent to a power estimation apparatus, estimates the squared magnitude of the modulated CDMA waveform envelope that would be formed by the baseband signals 114,116 after quadrature modulation, hereinafter referred to as the squared envelope magnitude, and outputs a signal representative of this squared envelope magnitude. The squared envelope magnitude predictor 202, according to this particular implementation, comprises a first squarer 216 that multiplies the I baseband signal 114 by itself, a second squarer 218 that multiplies the Q baseband signal 116 by itself, and an adder 220 that sums the outputs of the first and second squarers 216,218. The output from the adder 220 is a squared envelope magnitude corresponding to the baseband signals 114,116.

The multiplier 204 is utilized to establish a scaling threshold. The configurable threshold T is set to be one divided by the maximum acceptable envelope magnitude, as defined by the designer of the communication system, squared.

Subsequent to the actual squared envelope magnitude corresponding to the baseband signals 114,116 being produced within the squared envelope magnitude predictor 202 and input to the multiplier 204, the multiplier 204 generates a ratio u of the actual envelope magnitude squared and the maximum acceptable envelope magnitude squared.

This ratio u is input to the mapping table 206 which generates, with use of a mapping function f , a scaling factor by which the gain of the baseband signals 114,116 should be adjusted to ensure that there are no unwanted power peaks. The mapping function f is defined as follows:

$$f(u) = \begin{cases} 1 & u \leq 1 \\ \frac{1}{u} & u > 1 \end{cases}$$

If the ratio u is less than or equal to one, which indicates that the actual envelope magnitude is less than or equal to 5 the maximum acceptable envelope magnitude, a scaling factor $f(u)$ output from the mapping function f is set to one. If the ratio u is greater than one, indicating that the actual envelope magnitude is larger than the maximum acceptable envelope magnitude, the scaling factor $f(u)$, output from the 10 mapping function f , is set to a value sufficient to lower the power corresponding to the baseband signals 114,116 such that the actual envelope magnitude generated after modulation is equal to the maximum acceptable envelope magnitude. In this case, the output from the mapping table 206 is calculated by 15 taking the inversion of the square root of the ratio u , hence the scaling factor $f(u)$ would be equal to the maximum acceptable envelope magnitude divided by the prediction of the actual envelope magnitude. The mapping function f can be implemented using a look-up table or, alternatively, with the 20 use of logic circuits.

The mean power regulator 208 is not critical for the operation of the PPR block, but is an optional block utilized to maintain a mean output power for the Baseband PPR block 118 consistent with the mean input power, despite the 25 peak power spikes being scaled down. The mean power regulator 208, according to the particular implementation of FIGURE 2, comprises a squaring block 222 coupled in series with an average generator 223 and an inverted square root block 224, with the output of the inverted square root block 30 224 being input along with the output of the mapping table

206 into a multiplier 226.

The squaring block 222 is input with the scaling factor $f(u)$ generated within the mapping table 206 and generates an output $f^2(u)$ that corresponds to the scaling factor after being multiplied by itself, hereinafter referred to as a Squared Scaling Factor (SSF).

The average generator 223 functions to determine the average SSF generated at the squaring block 222. There are a number of possible implementations for the average generator 223. Within one embodiment, the average generator 223 sums N generated SSFs and subsequently divides the result by N , where N is the period of the average. In the implementation of FIGURE 2, the designer of the communication system inputs an Average Period Setting (APS) signal to the average generator 223 which determines the value for N . In an exemplary implementation of this average generator 223, a rotating window of dimension N is utilized that allows a continuous summing and dividing algorithm to proceed. In this algorithm, the newest generated SSF replaces the oldest generated SSF within the rotating window, hence maintaining the dimension of the window at N and ensuring the average SSF estimation is sufficiently accurate. Other implementations have an average generator 223 implemented with use of various types of LPFs.

The output signal from the average generator 223, representing the average SSF, is input to the inverted square root block 224. The square root block 224 outputs a signal corresponding to a square root of the inverted average of SSFs, hereinafter referred to as the inverted Root Mean Squared (RMS) scaling factors.

The inverted RMS scaling factors generated at the

inverted square root block 224 are multiplied in the multiplier 226 with the current scaling factor $f(u)$ output from the mapping table 206 to produce an instantaneous gain value that is input to each of the multipliers 212 in order 5 to scale the baseband signals 114,116. The instantaneous gain value is a ratio between the current scaling factor $f(u)$ and the RMS scaling factor and is used to scale both the I baseband signal 114 and the Q baseband signal 116. The results from the multipliers 212, in the implementation of 10 FIGURE 2, have all power peaks reduced and have the average output power consistent with the average input power. Without the use of the mean power regulator 208, the average output power from the Baseband PPR block 118 would be lower than the average input power since the power during periods 15 of power peaks would be reduced without adding additional power during periods of no power peaks. The mean power regulator 208 increases the instantaneous gain value at all times by the average reduction in power over all periods including peak power periods, hence fully compensating for 20 the reduction in average power.

The well understood LPF block 214, coupled to the outputs of the multipliers 212 is used to remove the out-of-band emissions caused by the processing within the Baseband PPR block 118. The delay block 210, coupled between 25 the baseband signals 114,116 and the multipliers 212, is used to delay the baseband signals such that the baseband signals 114,116 are exactly aligned with the instantaneous gain values produced by the multiplier 226.

One skilled in the art would understand that the 30 multiplier 204 combined with the mapping table 206 and possibly combined with the mean power regulator 208 can be

seen as a scaling factor generator. As well, it should be understood that the multipliers 212 and the LPF block 214 can be seen as a power scaling apparatus and a filtering apparatus respectively.

5 Although the description of the single carrier Baseband PPR block 118 depicted within FIGURE 2 is consistent with one implementation, it is recognized that modifications can be made. For example, as described previously, the mean power regulator 208 is removed within some alternative 10 embodiments. This results in the average output power from the Baseband PPR block 118 not necessarily being equal to the average input power. As well, a modification could be made in terms of the location of the square root operation within the mapping function f . An additional square root block in 15 one embodiment is included between the adder 220 and the multiplier 204. To adjust for this change, the configurable threshold signal T is redefined as one divided by the maximum acceptable envelope magnitude and the mapping function f within the mapping table 206 is adjusted to the following:

20

$$f(u) = \begin{cases} 1 & u \leq 1 \\ \frac{1}{u} & u > 1 \end{cases}$$

25 A multi-carrier CDMA transmitter, according to another embodiment of the present invention, using a Baseband PPR block is now described with reference to FIGURE 3. The multi-carrier transmitter is similar to the single carrier transmitter depicted within FIGURE 1, but the multi-carrier transmitter includes a plurality of pre-modulation carrier paths. In the example shown in FIGURE 3, a transmitter with 30 three carriers is depicted, though this is not meant to limit

the scope of the present invention.

Within this transmitter, three DSSs 302 generate three separate groups of data streams 304, each allowing transmission on multiple code channels corresponding to multiple users and/or multiple data streams for each user. These data streams 304 are encoded, spread, and combined within three respective CESSs 306 which each output respective I and Q baseband signals 308, 310. These baseband signals 308, 310 are then pulse shaped by three respective BPSFs 312, with all outputs being input to a multi-carrier Baseband PPR block 318, implementations of which are described in detail herein below with respect to FIGURES 4a, 4b and 9. Output from the multi-carrier Baseband PPR block 318 are three pairs of peak power reduced I and Q baseband signals 320, 322.

Subsequently, each pair of baseband signals 320, 322 are separately quadrature modulated within three respective QMs 324. The output signals 326 from the QMs 324 are input to a combiner 327 to generate a single compounded IF signal input to an UC 328 which shifts the frequency of the signal to the desired transmitting frequency. The up-converted signal 330 from the UC 328 is subsequently power amplified within a Multi-Carrier Power Amplifier (MCPA) 332, with the output signal 334 from the MCPA 332 being filtered by an RFF 336 before being transmitted to the air through an antenna 338.

It is understood that alternative embodiments of the multi-carrier transmitter, similar to those for the single carrier transmitter of FIGURE 1, are possible. As in the single carrier transmitter, the multi-carrier transmitter must have an additional stage for converting the signal from digital to analog format. For easier delay alignment, the preferred embodiment of the multi-carrier transmitter of

FIGURE 3 has the digital to analog conversion between the combiner 327 and the last up-conversion stage, but this should not limit the scope of the present invention.

A first implementation of the multi-carrier

5 Baseband PPR block 318 depicted within FIGURE 3 is described herein below with reference to FIGURE 4a. The overall concept is the same between the single carrier and multi-carrier Baseband PPR blocks 118,318, but the implementation requires modifications. The multi-carrier Baseband PPR block
10 318 comprises an envelope magnitude predictor 402 coupled in series with a multiplier 404, a mapping table 406, and a mean power regulator 408 within some embodiments; three delay blocks 410; six multipliers 412; and three LPF blocks 414, each LPF block comprising two LPFs.

15 The envelope magnitude predictor 402 takes as input the three pairs of baseband signals 314,316 output from the BPSFs 312. Each pair of baseband signals 314,316 is input to a pair of squarers 416,418 with the output of the squarers 416,418 being input to respective adders 419. Each set of squarers 416,418 and adders 419 are equivalent to the squared envelope magnitude predictor 202 depicted within FIGURE 2. The envelope magnitude predictor 402, within FIGURE 4a, further comprises three square root blocks 420 connected in series with the respective adders 419. The outputs from the 20 square root blocks 420 represent the envelope magnitude corresponding to their respective baseband signals 314,316 if the signals were modulated. These outputs are combined within adder 421 to generate a combined envelope magnitude approximation output from the envelope magnitude predictor 402. This approximation is representative of the worst case 25 magnitude of the envelope generated after all three baseband
30

5 pairs are quadrature modulated and combined. The magnitude prediction for each pair of baseband signals 314,316 generated with squarers 416,418, adders 419, and square root blocks 420 is a two dimensional estimation while the combination of the three individual envelope magnitude estimations is done linearly, as if the individual two dimensional estimations were lined up in phase perfectly. Hence, the final estimation, generated at the output of the adder 421, is the worst case of the individual baseband 10 envelope magnitudes lining up.

15 An alternative embodiment for the envelope magnitude predictor 402 is depicted in FIGURE 4b. This embodiment accounts for relative frequency and phase information to get an exact envelope magnitude prediction for the combined signal after quadrature modulation. This embodiment requires knowledge from the QMs 324, that being the frequency and phase that will be assigned to each carrier during quadrature modulation.

20 As shown within FIGURE 4b, one pair of baseband signals 314,316 are input to a complex mixer 428, another pair of baseband signals 314,316 are input to a complex mixer 430, and yet another pair of baseband signals 314,316 have the in-phase and quadrature signals input to in-phase and quadrature adders 432,434. In this example with three 25 carriers, the mixers 428,430 shift the frequency and phase of the baseband signals, so that they have the same relative frequency and phase that will occur in their respective QM outputs 326.

30 The in-phase signals output by complex mixers 428,430 are then input to the in-phase adder 432 and the quadrature signals output by the complex mixers 428,430 are

input to the quadrature adder 434. The outputs from the adders 432, 434 are input to in-phase and quadrature squarers 436, 438 respectively, with the outputs from the squarers 436, 438 being input to an adder 440. The output from the 5 adder 440 is input to a square root block 442 which produces the output to the alternative envelope magnitude predictor of FIGURE 4b. The output is an exact prediction of the envelope magnitude that the baseband signals 314, 316 would have produced at the output of combiner 327 if they were not scaled by the multi-carrier Baseband PPR block 318. The 10 prediction, in this case, takes into effect the difference in modulating frequency and phase for the different carriers and so is more accurate than that described within FIGURE 4a. The disadvantage of the envelope magnitude predictor of 15 FIGURE 4b is the increase in complexity.

In other embodiments, with different numbers of carriers, modifications to the envelope magnitude predictor 402 of FIGURE 4b can be contemplated. The key in any modification is to maintain the relative frequency and phase 20 between the signals so that the output of the envelope magnitude predictor 402 is an exact prediction of the envelope magnitude that the baseband signals 314, 316 would have produced at the output of combiner 327 if they were not scaled by the multi-carrier Baseband PPR block 318. In some 25 alternative embodiments, every pair of baseband signals has a complex mixer associated with it. As well, in some embodiments, the square root block 442 is removed and the square root function is implemented later within the multi-carrier Baseband PPR block 318.

30 Referring again to FIGURE 4a, the output from the envelope magnitude predictor 402 is input to the multiplier

404. Similar to that done for the single carrier PPR block 118 described with reference to FIGURE 2, the other input to the multiplier 404 is a configurable threshold signal T. The configurable threshold signal T, within FIGURE 4a, is

5 designed to be one over a predetermined maximum acceptable envelope magnitude, such that the output from the multiplier 404 is a ratio v between the actual approximation of the envelope magnitude and the maximum acceptable envelope magnitude.

10 The mapping table 406 is virtually identical to the mapping table of the single carrier PPR block of FIGURE 2, but the square root operation defined within the mapping function f of FIGURE 2 has been moved to within the envelope magnitude predictor 402. The mapping table 406 takes as

15 15 input the ratio v and contains a function g as follows:

$$g(v) = \begin{cases} 1 & v \leq 1 \\ \frac{1}{v} & v > 1 \end{cases}$$

20 Therefore, if the ratio v is less than or equal to one, which would indicate that the approximated envelope magnitude was less than or equal to the maximum acceptable envelope magnitude, a scaling factor g(v) output from the mapping table 406 would be one. If the ratio v was greater than one, representing the case that the approximation is greater than

25 the maximum acceptable envelope magnitude, then the scaling factor g(v) is set to a value sufficient to lower the power corresponding to the baseband signals 114, 116 to a power level such that the actual envelope magnitude generated after modulation and combination of the baseband signals 320, 322 is

30 equal to the maximum acceptable envelope magnitude. In this

case, the output from the mapping table 406 is one divided by the ratio v and this makes the scaling factor $g(v)$, similar to the scaling factor $f(u)$ in FIGURE 2, equal to the maximum acceptable envelope magnitude divided by the prediction of 5 the actual envelope magnitude. As well, the mapping table 406 can also be implemented with use of logic circuits with similar outcomes.

The mean power regulator, similar to that described for FIGURE 2, is an optional component of the PPR block 10 implementation being described with reference to FIGURE 4a. Similar to that described for FIGURE 2, the scaling factor $g(v)$, output from the mapping table 406, is input to the mean power regulator 408 along with an APS signal. The mean power regulator 408 comprises a squaring block 422, input with the 15 scaling factor $g(v)$, in series with an average generator 423 and an inverted square root block 424, with all three blocks functioning, in the implementation depicted within FIGURE 4a, as described above for the mean power regulator 208 within the single carrier Baseband PPR block 118. The outputs from 20 the inverted square root block 424 correspond to inverted RMS scaling factors. Further within the mean power regulator 408 is a multiplier 426, similar to multiplier 226 within FIGURE 2, that is input with the inverted RMS scaling factor from the inverted square root block 424 and the current scaling 25 factor $g(u)$ from the mapping table 406. The multiplier 426 generates an instantaneous gain value, similar to that generated by the multiplier 226 of FIGURE 2, input to each of the six multipliers 412.

The multipliers 412 are further input with delayed 30 versions of the baseband signals 314, 316 and output three pairs of peak power reduced baseband signals that are each

input to an individual LPF block 414. The LPF blocks 414 are designed to remove the out-of-band emissions caused by the processing within the Baseband PPR block 318. The delay blocks 410 generate the delayed baseband signals

5 corresponding to the baseband signals 314,316 that are input to the multipliers 412. As with the delay blocks 210 of FIGURE 2, the delay blocks 410 are used to exactly align the baseband signals 314,316 with their respective instantaneous gain values produced by multiplier 426.

10 The multi-carrier Baseband PPR block 318, depicted on FIGURE 4a, may be adapted to handle different numbers of carriers and is not limited to the case of three carriers as illustrated and described herein above. In cases that it is modified to handle only a single carrier, the implementation 15 is slightly different to that described with reference to FIGURE 2, but it is noted that either implementation would function properly.

20 Although the two implementations described herein above are for Baseband PPR blocks implemented prior to the modulation of the information signals, other embodiments are possible with the implementation of an Intermediate Frequency (IF) PPR block after the quadrature modulation stage within a transmitter. One implementation of a multi-carrier transmitter that utilizes such an IF PPR block is now 25 described with reference to FIGURES 5.

FIGURE 5 illustrates a transmitter with three carriers similar to that depicted in FIGURE 3, but with the Baseband PPR block 318 removed and an IF PPR block 504, implementations of which will be described herein below in 30 detail with reference to FIGURES 6, 7 and 11, added after the QMs 324. It would be understood by one skilled in the art

that the IF PPR block 504 could also be referred to as an envelope magnitude regulator. The change of the PPR blocks modifies the functioning of the transmitter slightly. The pulse shaped baseband signals 314,316, input to the Baseband 5 PPR block 318 in FIGURE 3, are now directly input to the QMs 324. Modulated IF outputs 502 from the QMs 324 are input to the IF PPR block 504 with envelope magnitude limited signals 506 subsequently being output to the combiner 327. In the implementation being described, the remaining components of 10 FIGURE 5 are identical to those described with reference to FIGURE 3. As in FIGURES 1 and 3, a conversion of the data information signals from digital to analog form is required that is not depicted within FIGURE 5. This conversion is preferably done after the IF PPR block 504, but before the 15 final up-conversion stage of the UC 328.

A first implementation of the IF PPR block 504, depicted in FIGURE 5, is now described with reference to FIGURE 6. This IF PPR block 504 comprises an adder 601, an envelope detector 602, a multiplier 604, a mapping table 606, 20 a mean power regulator 608 within an exemplary embodiment, three delay blocks 610, three multipliers 612, and three Bandpass Filters (BPFs) 614. The adder 601, input with each IF signal 502, outputs a combined IF signal to the envelope detector 602, that will be described in detail with reference 25 to FIGURE 7.

The output of the envelope detector 602 is an estimation of the envelope magnitude corresponding to the combination of the IF signals 502 and is input to the multiplier 604 along with a configurable threshold signal T . 30 The configurable threshold signal T is equal to one over a maximum acceptable envelope magnitude. Therefore, the output

of the multiplier 604 is a ratio v of the estimated overall envelope magnitude to the maximum acceptable envelope magnitude.

5 This ratio v is input to the mapping table 606 that is identical to the mapping table 406 within FIGURE 4a. This mapping table 606 comprises the mapping function g and outputs a scaling factor $g(v)$ as would be output from the mapping table 406.

10 Within an exemplary version of the IF PPR block of FIGURE 6, the mean power regulator 608 is utilized in similar fashion as described with mean power regulator 408 within FIGURE 4a. The mean power regulator 608 comprises squaring block 622 input with the scaling factor $g(v)$, average generator 623 input with the output from the squaring block 15 622 and an APS signal, an inverted square root block 624 input with the output from the average generator 623, and a multiplier 626 input with the current scaling factor $g(v)$ from the mapping table 606 and the inverted RMS scaling factor output from the inverted square root block 624. All 20 of these components within the mean power regulator 608 operate identically to those within the mean power regulator 408 of FIGURE 4a.

The output from the multiplier 626 is an instantaneous gain value that is input to the multipliers 612 25 in order to scale the modulated IF signals 502. The multipliers 612 are input with delayed versions of the IF signals 502 and output signals that have high envelope magnitudes reduced and average power unchanged. Each output from the multipliers 612 is input to one of the BPFs 614 30 which subsequently filters the out-of-band emissions generated through the processing within the IF PPR block 504.

The delay blocks 610 are utilized, as in FIGURES 2 and 4a, to delay the input signals to the IF PPR block 504, in this case the IF signals 502, such that the inputs to the multipliers 612 are exactly aligned with the corresponding 5 instantaneous gain values generated at the multiplier 626.

It is noted that the implementation depicted in FIGURES 5 and 6 is only one possible implementation of a transmitter utilizing an IF PPR block. Other embodiments are possible that have the IF PPR block anywhere between the QMs 10 324 and the MCPA 332 with only slight modifications required within the IF PPR block 504. As well, although not shown, a single carrier transmitter utilizing a single carrier IF PPR block is possible by simply scaling FIGURES 5 and 6 to a single carrier with the combiner 327 in FIGURE 5 and the 15 combiner 601 in FIGURE 6 removed.

There are numerous implementations for the envelope detector 602 within FIGURE 6. One sample implementation of the envelope detector 602, now described with reference to FIGURE 7, comprises an optional Up-Sampling and Interpolation (USI) block 702 coupled in series with an absolute value block 704 and a Maximum Value Over Time (MVOT) block 706. In a digital implementation, as described in FIGURE 6, the optional USI block 702 may be included within the implementation of the envelope detector 602 in order to 20 increase its accuracy. This increase in accuracy is dependent on the sampling rate relative to the carrier 25 frequency.

The absolute value block 704 utilizes a rectifier to take the absolute value of the bipolar IF signal input 30 from the USI block 702. The rectifier, in a digital implementation, is a logic circuit performing the following

function:

$$y(x) = \begin{cases} x & x \geq 0 \\ -x & x < 0 \end{cases}$$

5 where x is in the input and y is the output. The MVOT block 706, is a well understood block which measures the maximum value output from the absolute value block 704 over a predetermined time period Ta. For good accuracy, Ta should be larger than one cycle of the IF signals 502, preferably 10 significantly larger than the sampling rate of the MVOT block 706, and significantly less than 1/W, where W is the signal bandwidth of the signals 502.

15 The first implementations for a single carrier Baseband PPR block, a multi-carrier Baseband PPR block and a multi-carrier IF PPR block as described above with reference to FIGURES 2, 4a and 6 operate with one common disadvantage.

20 Although these PPR blocks operate to reduce the incidence of peak power spikes by multiplying delayed versions of the input signals by corresponding scaling factors and subsequently filtering the scaled signals, the filtering operation unfortunately is performed on all signals; whether the input signals required scaling or not. The passband ripple of the filtering apparatus within each of the implementations discussed above will distort all the signals 25 passing through the PPR blocks, resulting in errors within both input signals that required scaling and those that were below the power threshold level required. Implementations of the PPR blocks 118, 318, 504 are described herein below with reference to FIGURES 8a, 8b, 9 and 10 according to the 30 present invention which mitigate this problem with the above described implementations.

FIGURE 8a illustrates a second implementation of the Baseband PPR block 118 implemented within the single carrier transmitter depicted in FIGURE 1. Similar to the first implementation of FIGURE 2, the single carrier Baseband 5 PPR block of FIGURE 8a utilizes nonlinear baseband processing to instantaneously scale the pulse shaped I and Q CDMA baseband signals 114,116 to within an acceptable threshold range. One important difference between these two implementations, as will be described below, is the removal 10 of the LPF block from the primary signal path so that Baseband signals that do not require PPR scaling are not deteriorated through unnecessary filtering.

The Baseband PPR block 118, depicted within FIGURE 8a, comprises a first delay block 802 input with the I and Q 15 baseband signals 114,116 and coupled in series with a second delay block 804 and a set of two differential adders 806 that generate the baseband outputs 120,122 which are subsequently input to the QM 124. Further, the Baseband PPR block of FIGURE 8a comprises the squared envelope magnitude predictor 20 202 input with the I and Q baseband signals 114,116; the multiplier 204 input with the output from the squared envelope magnitude predictor 202 and a configurable threshold signal T; the mapping table 206 input with the output from the multiplier 204; a differential adder 808 input with a 25 value of one along with the output from the mapping table 206; a set of two multipliers 810 input with the outputs from the first delay block 802 and the output from the differential adder 808; and a Lowpass Filter (LPF) block 812 input with the outputs from the set of multipliers 810 and 30 further coupled to the set of differential adders 806. In this case, the LPF block comprises two LPFs, one for each of

the outputs from the multipliers 810.

In the implementation illustrated in FIGURE 8a, the squared envelope magnitude predictor 202, the multiplier 204 and the mapping table 206 all operate in the same manner as 5 previously described above for the implementation of FIGURE 2. The squared envelope magnitude predictor 202 estimates the squared magnitude of the modulated CDMA waveform envelope that would be formed by the baseband signals 114, 116 after quadrature modulation and outputs a signal representative of 10 this squared envelope magnitude. The multiplier 204 receives this signal representative of the squared envelope magnitude and compares it with a scaling threshold T . As described previously for FIGURE 2, the configurable threshold T is set to be one divided by the maximum acceptable envelope 15 magnitude, as defined by the designer of the communication system, squared so that the multiplier generates a ratio u of the actual envelope magnitude squared and the maximum acceptable envelope magnitude squared. This ratio u is input to the mapping table 206 which generates, with use of the 20 mapping function f described previously for FIGURE 2, a scaling factor $f(u)$.

The scaling factor $f(u)$ is subsequently input to the differential adder 808 along with a value of one. The output from the differential adder is an expression for one 25 subtracted by the scaling factor, that being $1 - f(u)$. If the scaling factor is equal to one, as would be the case in which the actual envelope magnitude squared is less than or equal to the maximum acceptable envelope magnitude squared, the output from the differential adder 808 would be zero. 30 Alternatively, if the scaling factor is less than one, as would be the case in which the actual envelope magnitude

squared is greater than the maximum acceptable envelope magnitude squared, the output from the differential adder 808 would be equal to a value between 0 and 1 which represents the percentage (in decimal form) by which the input signals' 5 estimated envelope magnitude must be reduced to equal the maximum acceptable envelope magnitude.

Each of the multipliers 810 receives the output from the differential adder 808 along with a delayed version of one of the input signals 114,116 from the first delay 10 block 802. The first delay block 802 is used to delay the baseband signals 114,116 so that they are exactly aligned with the instantaneous outputs of the differential adder 808, hence compensating for the delays within components 202,204,206 and 808. The outputs from the multipliers 810, 15 hereinafter referred to as excess power correction signals, represent the amount in which the input signals should be reduced in order to ensure that their power peaks above the threshold level are removed. In this case, if the output from the differential adder 808 equals zero, then the excess 20 power correction signal output from the multipliers 810 is null as well; this indicating that no reduction in power within the baseband signals is required. If the output from the differential adder 808 is a value between 0 and 1, then the excess power correction signals output from the 25 multipliers 810 are representative of the portions of the input signals 114,116 that are above the threshold power level.

The LPF block 812 comprises two individual LPFs that each receive one of the excess power correction signals 30 output from the multipliers 810. These LPFs are utilized to remove the out-of-band emissions generated within the excess

power correction signals during the processing within the multipliers 810. As depicted within FIGURE 8a, the filtered outputs of the LPF block 812, hereinafter referred to as filtered excess power correction signals, are input to

5 corresponding ones of the differential adders 806 along with delayed versions of the corresponding ones of the input signals 114,116 from the second delay block 804. The second delay block 804 is used to delay the previously delayed versions of the baseband signals 114,116 from the first delay
10 block 802 so that they are exactly aligned with the instantaneous filtered excess power correction signals output from the LPF block 812, hence compensating for the delays within components 810 and 812. Within the implementation of FIGURE 8a, each of the differential adders 806 operates to
15 subtract the delayed version of one of the input signals 114,116 from its corresponding filtered excess power correction signal. The results of these subtraction operations of FIGURE 8a are the baseband outputs 120,122, the baseband outputs 120,122 being excess peak power reduced
20 versions of the corresponding baseband inputs 114,116. It is noted that if no power scaling of the baseband inputs 114,116 is required, the differential adders 806 subtract only a null signal from the delayed versions of the signals. Thus, no change is made to the baseband inputs that do not require
25 power scaling.

Although the description of FIGURE 8a has been described above for one particular implementation, this should not limit the scope of the present invention. It should be understood that the alternative implementations
30 described above for the squared envelope magnitude predictor 202, the multiplier 204 and the mapping table 206 of FIGURE 2

also apply as alternatives within the implementation of FIGURE 8a. For instance, similar to the implementation described above, it should be recognized that the mapping function f could be implemented using a look-up table or,
5 alternatively, with the use of logic circuits.

Further, a mean power regulator similar to mean power regulator 208 of FIGURE 2 could be implemented within FIGURE 8a in some embodiments. This mean power regulator could be implemented between the mapping table 206 and the
10 differential adder 808. Similar to the apparatus within FIGURE 2, a mean power regulator within FIGURE 8a could be utilized to maintain a mean output power for the Baseband PPR block consistent with the mean input power, despite the peak power spikes being scaled down. If a mean power regulator is
15 implemented within FIGURE 8a it could be implemented as described above with reference to FIGURE 2, though the implementation of the mean power regulator should not be limited to such a design.

Yet further, the square root function that is
20 incorporated within the mapping table 206 of FIGURE 8a could be moved. For instance, an alternative implementation for these components is illustrated within FIGURE 8b in which the square root function has been moved prior to the mapping table 206. Within FIGURE 8b, all of the components of the
25 single carrier Baseband PPR block 118 are the same as those described above for the design in FIGURE 8a, but with an envelope magnitude predictor 814 replacing the squared envelope magnitude predictor 202 of FIGURE 8a. In this case, the envelope magnitude predictor comprises the first and
30 second squarers 216,218 and the adder 220 similar to the predictor 202 but further comprises a square root operator

816 coupled to the output of the adder 220. The square root operator 816 receives the signal representative of the squared envelope magnitude and outputs a signal representative of the actual envelope magnitude. To adjust 5 for this change in location of the square root function, the configurable threshold signal T is redefined as one divided by the maximum acceptable envelope magnitude for this implementation. Further, the mapping function f within the mapping table 206 is adjusted to the following as described 10 above with reference to the alternatives to the PPR block of FIGURE 2:

$$f(u) = \begin{cases} 1 & u \leq 1 \\ \frac{1}{u} & u > 1 \end{cases}$$

15 One skilled in the art would understand that the multiplier 204 combined with the mapping table 206 and possibly combined with a mean power regulator can be seen as a scaling factor generator. Further, it should be understood that the differential adder 808 combined with multipliers 810 20 can be seen as an excess power correction generator, the LPF block 812 can be seen as a filtering apparatus and the differential adders 806 can be seen as an excess power removal apparatus.

Now turning to the multi-carrier transmitter of 25 FIGURE 3, FIGURE 9 illustrates a second implementation of the multi-carrier Baseband PPR block 318. Similar to the first implementation of FIGURE 4a, the multi-carrier Baseband PPR block of FIGURE 9 utilizes nonlinear baseband processing to instantaneously scale the three pairs of baseband signals 30 314, 316 to within an acceptable threshold range. Similar to

FIGURES 8a and 8b, one important difference between the implementation of FIGURE 9 and that of FIGURE 4a, as will be described below, is the removal of the LPF blocks from the primary signal paths so that Baseband signals that do not 5 require PPR scaling are not deteriorated through unnecessary filtering.

The multi-carrier Baseband PPR block 318, depicted within FIGURE 9, comprises three first delay blocks 902 input with respective ones of the three pairs of baseband signals 10 314,316 and coupled in series with three corresponding second delay blocks 904 and a set of six corresponding differential adders 906 that generate the three pairs of baseband outputs 320,322 which are subsequently input to their corresponding QMs 324. Further, the Baseband PPR block of FIGURE 9 15 comprises the envelope magnitude predictor 402 input with the three pairs of baseband signals 314,316; the multiplier 404 input with the output from the squared envelope magnitude predictor 402 and a configurable threshold signal T; the mapping table 406 input with the output from the multiplier 20 404; a differential adder 908 input with a value of one along with the output from the mapping table 406; a set of six multipliers 910 input with corresponding outputs from the first delay blocks 902 along with the output from the differential adder 908; and three Lowpass Filter (LPF) blocks 25 912 input with corresponding outputs from the set of multipliers 910 and further coupled to corresponding ones of the set of differential adders 906. In this case, each of the LPF blocks 912 comprise two LPFs, one for each of the outputs from the multipliers 910.

30 In the implementation illustrated in FIGURE 9, the envelope magnitude predictor 402, the multiplier 404 and the

mapping table 406 all operate in the same manner as previously described above for the implementation of FIGURE 4a. The envelope magnitude predictor 402 generates a combined envelope magnitude approximation that is

5 representative of the worst case magnitude of the envelope generated after all three baseband pairs are quadrature modulated and combined. The multiplier 404 receives this combined envelope magnitude approximation and compares it with a scaling threshold T . As described previously for
10 FIGURE 4a, the configurable threshold T is set to be one divided by the maximum acceptable envelope magnitude, as defined by the designer of the communication system, so that the multiplier generates a ratio v of the approximation of the actual envelope magnitude and the maximum acceptable
15 envelope magnitude. This ratio v is input to the mapping table 406 which generates, with use of the mapping function g described previously for FIGURE 4a, a scaling factor $g(v)$.

The scaling factor $g(v)$ is subsequently input to the differential adder 908 along with a value of one.

20 Similar to that described above for FIGURE 8a, the output from the differential adder 908 is an expression for one subtracted by the scaling factor, that being $1 - g(v)$. If the scaling factor is equal to one, as would be the case in which the approximation of the actual envelope magnitude is
25 less than or equal to the maximum acceptable envelope magnitude, the output from the differential adder 908 would be zero. Alternatively, if the scaling factor is less than one, as would be the case in which the approximation of the actual envelope magnitude is greater than the maximum
30 acceptable envelope magnitude, the output from the differential adder 908 would be equal to a value between 0

and 1 which represents the percentage (in decimal form) by which the combined input signals' estimated envelope magnitude must be reduced to equal the maximum acceptable envelope magnitude.

5 Each of the six multipliers 910 receives the output from the differential adder 908 along with a delayed version of a corresponding one of the input signals 314,316 from the first delay block 902. The first delay block 902 is used to delay the three pairs of baseband signals 314,316 so that
10 they are exactly aligned with the instantaneous outputs of the differential adder 908, hence compensating for the delays within components 402,404,406 and 908. The outputs from the multipliers 910, hereinafter referred to as excess power correction signals, represent the amount in which each of the
15 input signals should be reduced in order to ensure that any possible power peaks above the threshold level caused when the pairs of baseband signals are combined are removed. In this case, if the output from the differential adder 908 equals zero, then the excess power correction signal output
20 from the multipliers 910 is null as well; this indicating that no reduction in power within the baseband signals is required. If the output from the differential adder 908 is a value between 0 and 1, then the excess power correction signals output from the multipliers 910 are representative of
25 the portions of the three pairs of input signals 314,316 that possibly could be above the threshold power level when combined.

Each of the three LPF blocks 912 comprise two individual LPFs that each receive a corresponding one of the
30 excess power correction signals output from the multipliers 910. Similar to the LPFs of FIGURE 8a, the LPFs of FIGURE 9

are utilized to remove the out-of-band emissions generated within the excess power correction signals during the processing within the multipliers 910. As depicted within FIGURE 9, the filtered outputs of the LPF blocks 912,

5 hereinafter referred to as filtered excess power correction signals, are input to corresponding ones of the differential adders 906 along with delayed versions of the corresponding ones of the input signals 314,316 from the second delay block 904. The second delay block 904 is used to delay the
10 previously delayed versions of the three pairs of baseband signals 314,316 from the first delay block 902 so that they are exactly aligned with the instantaneous filtered excess power correction signals output from the LPF blocks 912, hence compensating for the delays within components 910 and
15 912. Within the implementation of FIGURE 9, each of the differential adders 906 operates to subtract the delayed version of one of the input signals 314,316 from its corresponding filtered excess power correction signal. The results of these subtraction operations of FIGURE 9 are the
20 three pairs of baseband outputs 320,322. Much like that described above for FIGURE 8a, if no power scaling of the pairs of baseband inputs 314,316 is required, the differential adders 906 subtract only a null signal from the delayed versions of the signals. Thus, no change is made to
25 the pairs of baseband inputs that do not require power scaling.

Although the description of FIGURE 9 has been described above for one particular implementation, this should not limit the scope of the present invention. It
30 should be understood that the alternative implementations described above for the envelope magnitude predictor 402, the

multiplier 404 and the mapping table 406 of FIGURE 4a also apply as alternatives within the implementation of FIGURE 9. For instance, similar to the implementation described above, it should be recognized that the mapping function g could be 5 implemented using a look-up table or, alternatively, with the use of logic circuits.

Further, a mean power regulator similar to mean power regulator 408 of FIGURE 4a could be implemented within FIGURE 9 in some embodiments. This mean power regulator 10 could be implemented between the mapping table 406 and the differential adder 908. Similar to the apparatus within FIGURE 4a, a mean power regulator within FIGURE 9 could be utilized to maintain a mean output power for the Baseband PPR block consistent with the mean input power. If a mean power 15 regulator is implemented within FIGURE 9 it could be implemented as described above with reference to FIGURE 4a, though the implementation of the mean power regulator should not be limited to such a design.

20 Yet further, the alternative embodiment for the envelope magnitude predictor 402 depicted in FIGURE 4b could further be applied within the PPR block of FIGURE 9. As described above, this embodiment accounts for relative frequency and phase information to get an exact envelope magnitude prediction for the combined signal after quadrature 25 modulation. This embodiment requires knowledge from the QMs 324, that being the frequency and phase that will be assigned to each carrier during quadrature modulation. As discussed above, a disadvantage of the envelope magnitude predictor of FIGURE 4b is the increase in complexity.

30 The multi-carrier Baseband PPR block 318, depicted in FIGURE 9, may be adapted to handle different numbers of

carriers and is not limited to the case of three carriers as illustrated and described herein above. In cases that it is modified to handle only a single carrier, the implementation is slightly different to that described with reference to 5 FIGURE 8a, but it is noted that either implementation would function properly.

One skilled in the art would understand that the multiplier 404 combined with the mapping table 406 and possibly combined with a mean power regulator can be seen as 10 a scaling factor generator. Further, it should be understood that the differential adder 908 combined with multipliers 910 can be seen as an excess power correction generator, the LPF block 912 can be seen as a filtering apparatus and the differential adders 906 can be seen as an excess power 15 removal apparatus.

Another technique according to the present invention for performing peak power reduction within a multi-carrier transmitter is to input the baseband input signals 314, 316 into a multi-carrier combiner 1000 in order to 20 generate combined single carrier baseband signals 114, 116 that can be subsequently input to a single carrier Baseband PPR block 118 such as that described previously with respect to FIGURES 2, 8a and 8b. FIGURE 10 illustrates a possible implementation for such a multi-carrier combiner 1000. In 25 this case, complex mixers 428, 430 and in-phase and quadrature adders 432, 434 are implemented in the same manner as described previously for FIGURE 4b. The outputs of the in-phase and quadrature adders 432, 434 in this case are the in-phase and quadrature baseband signals 114, 116 that can be 30 input within the single carrier Baseband blocks of FIGURES 2, 8a or 8b. In the embodiment of the present invention in

which the multi-carrier combiner 1000 is coupled to the single carrier Baseband PPR block 118 of one of FIGURES 2, 8a, or 8b, a modified transmitter design is required. In this design, as depicted within FIGURE 11, the transmitter 5 comprises DSS 302, CESs 306 and BPSFs 312 as described previously for FIGURE 3, the BPSFs being coupled to the multi-carrier combiner 1000. The multi-carrier combiner 1000 is coupled to the Baseband PPR block 118 which is further coupled to the QM 124, UC 128, MCPA 132, the RFF 136 and the 10 antenna 138 as previously described with reference to FIGURE 1.

It should be understood that alternative implementations of the multi-carrier combiner 1000 of FIGURE 10 are possible. For instance, the alternative embodiments 15 of the components 428, 430, 432, 434 described previously further apply to the multi-carrier combiner 1000.

Now turning to the transmitter of FIGURE 5, a second implementation of the IF PPR block 504 is now described with reference to FIGURE 12. Similar to the first 20 implementation of FIGURE 6, the IF PPR block of FIGURE 12 utilizes nonlinear baseband processing to instantaneously scale the three carrier signals 502 to within an acceptable threshold range. Similar to FIGURES 8a, 8b and 9, one important difference between the implementation of FIGURE 12 25 and that of FIGURE 6, as will be described below, is the removal of the LPF blocks from the primary signal paths so that IF signals that do not require PPR scaling are not deteriorated through unnecessary filtering.

The IF PPR block 504, depicted within FIGURE 12, 30 comprises three first delay blocks 1202 input with respective ones of the three IF signals 502 and coupled in series with

three corresponding second delay blocks 1204 and a set of three corresponding differential adders 1206 that generate the three IF outputs 506 which are subsequently input to combiner 327. Further, the IF PPR block of FIGURE 12

5 comprises the adder 601 input with the three IF input signals 502; the envelope detector 602 input with the output of the adder 601; the multiplier 604 input with the output from the envelope detector 602 and a configurable threshold signal T; the mapping table 606 input with the output from the
10 multiplier 604; a differential adder 1208 input with a value of one along with the output from the mapping table 606; a set of three multipliers 1210 input with corresponding outputs from the first delay blocks 1202 along with the output from the differential adder 1208; and three Bandpass
15 Filter (BPF) blocks 1212 input with corresponding outputs from the set of multipliers 1210 and further coupled to corresponding ones of the set of differential adders 1206. In this case, each of the BPF blocks 1212 comprise a single BPF.

20 In the implementation illustrated in FIGURE 12, the adder 601, the envelope detector 602, the multiplier 604 and the mapping table 606 all operate in the same manner as previously described above for the implementation of FIGURE 6. The adder 601, input with each IF signal 502, outputs a
25 combined IF signal to the envelope detector 602. The envelope detector which could be implemented as described above with reference to FIGURE 7, outputs an estimation of the envelope magnitude corresponding to the combination of the IF signals 502. The multiplier 604 receives this
30 estimation of the envelope magnitude and compares it with a scaling threshold T. As described previously for FIGURE 6,

the configurable threshold T is set to be one divided by the maximum acceptable envelope magnitude, as defined by the designer of the communication system, so that the multiplier 604 generates a ratio v of the estimated overall envelope

5 magnitude to the maximum acceptable envelope magnitude. This ratio v is input to the mapping table 606 which generates, with use of the mapping function g described previously for FIGURES 4a and 6, a scaling factor g(v).

The scaling factor g(v) is subsequently input to
10 the differential adder 1208 along with a value of one.

Similar to that described above for FIGURES 8a and 9, the output from the differential adder 1208 is an expression for one subtracted by the scaling factor, that being $1 - g(v)$.

15 If the scaling factor is equal to one, as would be the case in which the approximation of the actual envelope magnitude is less than or equal to the maximum acceptable envelope magnitude, the output from the differential adder 1208 would be zero. Alternatively, if the scaling factor is less than one, as would be the case in which the approximation of the
20 actual envelope magnitude is greater than the maximum acceptable envelope magnitude, the output from the differential adder 1208 would be equal to a value between 0 and 1 which represents the percentage (in decimal form) by which the combined input signals' estimated envelope
25 magnitude must be reduced to equal the maximum acceptable envelope magnitude.

Each of the three multipliers 1210 receives the output from the differential adder 1208 along with a delayed version of a corresponding one of the IF input signals 502
30 from the first delay block 1202. The first delay block 1202 is used to delay the three IF signals 502 so that they are

exactly aligned with the instantaneous outputs of the differential adder 1208, hence compensating for the delays within components 601, 602, 604, 606 and 1208. The outputs from the multipliers 1210, hereinafter referred to as excess power 5 correction signals, represent the amount in which each of the input signals should be reduced in order to ensure that any possible power peaks above the threshold level caused when the IF signals are combined are removed. In this case, if the output from the differential adder 1208 equals zero, then 10 the excess power correction signal output from the multipliers 1210 is null as well; this indicating that no reduction in power within the IF input signals 502 is required. If the output from the differential adder 1208 is a value between 0 and 1, then the excess power correction 15 signals output from the multipliers 1210 are representative of the portions of the three IF signals 502 that possibly could be above the threshold power level when combined.

Each of the three LPF blocks 1212 comprise a single LPF that receives a corresponding one of the excess power 20 correction signals output from the multipliers 1210. Similar to the LPFs of FIGURES 8a and 9, the LPFs of FIGURE 12 are utilized to remove the out-of-band emissions generated within the excess power correction signals during the processing 25 within the multipliers 1210. As depicted within FIGURE 12, the filtered outputs of the LPF blocks 1212, hereinafter referred to as filtered excess power correction signals, are input to corresponding ones of the differential adders 1206 along with delayed versions of the corresponding ones of the IF input signals 502 from the second delay block 1204. The 30 second delay block 1204 is used to delay the previously delayed versions of the three IF input signals 502 from the

first delay block 1202 so that they are exactly aligned with the instantaneous filtered excess power correction signals output from the LPF blocks 1212, hence compensating for the delays within components 1210 and 1212. Within the

5 implementation of FIGURE 12, each of the differential adders 1206 operates to subtract the delayed version of one of the input signals 502 from its corresponding filtered excess power correction signal. The results of these subtraction operations of FIGURE 12 are the three IF output signals 506.

10 Much like that described above for FIGURES 8a and 9, if no power scaling of the IF input signals 502 is required, the differential adders 1206 subtract only a null signal from the delayed versions of the signals. Thus, no change is made to the IF input signals that do not require power scaling.

15 Although the description of FIGURE 12 has been described above for one particular implementation, this should not limit the scope of the present invention. It should be understood that the alternative implementations described above for the envelope detector 602, the multiplier 20 604 and the mapping table 606 of FIGURE 6 also apply as alternatives within the implementation of FIGURE 12. For instance, similar to the implementation described above, it should be recognized that the mapping function g could be implemented using a look-up table or, alternatively, with the 25 use of logic circuits.

Further, a mean power regulator similar to mean power regulator 608 of FIGURE 6 could be implemented within FIGURE 12 in some embodiments. This mean power regulator could be implemented between the mapping table 606 and the 30 differential adder 1208. Similar to the apparatus within FIGURE 6, a mean power regulator within FIGURE 12 could be

utilized to maintain a mean output power for the IF PPR block consistent with the mean input power. If a mean power regulator is implemented within FIGURE 12 it could be implemented as described above with reference to FIGURE 6, 5 though the implementation of the mean power regulator should not be limited to such a design.

Yet further, as discussed above with reference to FIGURE 6, it is noted that other embodiments of transmitters are possible that have the IF PPR block anywhere between the 10 QMs 324 and the MCPA 332 with only slight modifications required within the IF PPR block 504 of FIGURE 12. As well, although not shown, a single carrier transmitter utilizing a single carrier IF PPR block is possible by simply scaling the IF PPR block 504 of FIGURE 12 to a single carrier with the 15 combiner 601 removed. Further, the IF PPR block 504, depicted in FIGURE 12, may be adapted to handle different numbers of carriers and is not limited to the case of three carriers as illustrated and described herein above.

One skilled in the art would understand that the 20 multiplier 604 combined with the mapping table 606 and possibly combined with a mean power regulator can be seen as a scaling factor generator. Further, it should be understood that the differential adder 1208 combined with multipliers 1210 can be seen as an excess power correction generator, the 25 LPF block 1212 can be seen as a filtering apparatus and the differential adders 1206 can be seen as an excess power removal apparatus.

There are numerous advantages to the 30 implementations of the PPR blocks of FIGURES 8a, 8b, 9 and 12, according to the present invention described above. For one, as described above, if no power scaling of the input

signals is required, the respective differential adders 806, 906, 1206 subtract only a null signal from the delayed versions of the signals. Thus, no significant change is made to the inputs that do not require power scaling. In the 5 implementations of the PPR blocks of FIGURES 2, 4a and 6, all signals, whether requiring scaling or not, are filtered by respective filtering apparatus 214, 414, 614. This filtering can deteriorate the quality of these signals by adding an error component. In the implementation of FIGURES 8a, 8b, 9 10 and 12, the respective filtering apparatus 812, 912, 1212 may add a small error to the excess power correction signals, but these correction signals are error correction signals themselves. It is much less damaging to add a slight error to an error signal than to add a slight error to the 15 fundamental signal. Within the PPR blocks of FIGURES 8a, 8b, 9 and 12, no significant error would be added to input signals that do not require scaling and, any error that is added to input signals that do require scaling, is less than the possible error added via the first implementations of 20 these PPR blocks described above with reference to FIGURES 2, 4a and 6.

Another advantage of the second implementations of the PPR blocks of FIGURES 8a, 8b, 9 and 12 is the possibility to reduce the quality of the filtering apparatus that are 25 utilized. For similar reasons as discussed above, the error added to the excess power correction signals by the filtering apparatus within these implementations is not as critical as error added to the actual baseband or IF signals by filtering apparatus within the implementations of FIGURES 2, 4a and 6. 30 The reduced quality requirement within the filtering apparatus allows for a reduced number of bits to be used

within the LPFs and BPFs of these apparatus. The reduction in number of bits can reduce the cost of the filters by reducing the number of multipliers and, if the filter design have filters in series, the removal of multipliers could 5 further increase the speed of the filtering apparatus.

It should be noted that although the second implementations of the PPR blocks described above with reference to FIGURES 8a, 8b, 9 and 12 have their filtering apparatus operating on the excess power correction signals, 10 this should not limit the scope of the present invention. For instance, the filtering apparatus could be moved to the output of the differential adders 806, 906, 1206 within these figures, though it is recognized that this would mute the above described advantages for the second implementations of 15 the PPR blocks.

All of the implementations of the PPR blocks described above which utilize power gain scalers further have advantages over other implementations that utilize hard power limiters. For digital implementations of PPR blocks in which 20 a hard limiter is utilized rather than the scaling implementation of the above described implementations, the hard limiter would create strong harmonics while limiting the power. These strong harmonics would fall back to the Nyquist band and cause significant distortions. As well, a hard 25 limiter must operate with the combined multi-carrier signals.

Thus, after the hard limiter operation, the IF signals cannot be individually filtered resulting in inter-carrier distortions caused by the hard limiter not being removed.

There are numerous further advantages gained within 30 the transmitter that utilizes a PPR block according to the present invention. The PPR block scales down the peak power

periods while, in the embodiments that utilize a mean power regulator, the PPR block further maintains the average power level, therefore reducing the CDMA Peak-to-Average Power Ratio (PAPR). This reduced PAPR is a significant advantage 5 of the present invention and results in the PA, within the transmitter, being capable of operating at higher average power levels while still satisfying the out-of-band emissions requirements.

Another advantage of the present invention is the 10 flexibility that this implementation has in terms of supporting various numbers of active carriers. In the three carrier examples depicted within FIGURES 4a, 6, 9, 10 and 12 any of the three carriers can be active or inactive with arbitrary relative transmit power between them.

15 Although the implementations described above are designed to reduce the peak power spikes within input signals to the PPR blocks, it should be noted that the output signals of the PPR blocks may not necessarily have power levels that are consistent with envelope magnitudes less than the maximum acceptable envelope magnitude. This is due to the operation 20 of the filtering apparatus. While the filters remove out-of-band emissions from the excess power correction signals in FIGURES 8a, 8b, 9 and 12 and remove out-of-band emissions from the multiplied signals in FIGURES 2, 4a and 6, the 25 filters also generally slightly increase the power of the peak power spike. For instance, while the entire peak power spikes might be removed if the filtering apparatus was not within the PPR blocks described above, with the filtering apparatus, the peak power spikes may be only reduced by a 30 particular percentage, such as 80%.

To overcome this limitation in the design of the

PPR blocks described above, alternatives to the implementations of the PPR blocks of FIGURES 2, 4a, 6, 8a, 9 or 12 include a PPR block coupled in series with at least one other PPR block. This coupling of multiple PPR blocks in a 5 cascaded fashion helps to further remove any new peak power spikes that are rebuilt by the filters within the respective PPR blocks.

Although the different embodiments of the present invention depicted herein above have different 10 implementations for the envelope magnitude predictor, it should be understood that the output signal from the envelope magnitude predictor, hereinafter referred to as the overall input power estimation signal, has the magnitude estimation of the overall input power level incorporated within it. 15 This does not necessarily mean that the overall input power estimation signal is equal to the overall input power estimation level, but that it is possibly a manipulated version of the overall power estimation level using a monotonic function. For example, FIGURE 2 depicts a case 20 where the overall input power estimation signal is the estimated overall input power level squared. Similarly, a maximum acceptable power signal incorporates the maximum acceptable power level, previously described as the maximum acceptable envelope magnitude, but does not necessarily mean 25 that the maximum acceptable power signal is equal to the maximum acceptable power level.

Depending on the designer's selection of the configurable threshold signal T and the analog power amplifier drive level, the PPR block can be utilized for a 30 number of different purposes. Four different setups for utilizing PPR blocks are now described, these setups are

hereinafter referred to as modes A through D.

Within mode A, the average output power of the power amplifier remains constant, with the addition of the PPR block simply reducing the out-of-band emissions while not degrading the in-band waveform quality. In this mode, the PPR block is set using the configurable threshold signal T to clip the information signal no more than the power amplifier would have clipped if the PPR block were not utilized. Only the location of the clipping changes to an earlier stage.

Because the LPF(s) within the PPR block removes the out-of-band emissions caused by the PPR scaling and less out-of-band emissions are generated by the power amplifier because of the PPR block, the overall out-of-band emissions are reduced.

Within mode B, the out-of-band emissions are

further improved from that of mode A while the same average output power level is used, resulting in a slight degradation of the in-band waveform quality. In this mode, the PPR block clipping depth is increased beyond that originally clipped by the power amplifier without the PPR block. This is done by

decreasing the maximum acceptable envelope magnitude as incorporated within the configurable threshold signal T. The combined amount of clipping performed by this setup from the PPR block and the power amplifier is higher than that performed by the power amplifier alone. This reduction in out-of-band emissions is done at a cost within the in-band waveform quality.

Within mode C, the out-of-band emissions are decreased at the same time the average output power from the power amplifier is increased, causing a degradation in the in-band waveform quality to a minimum acceptable level. In this mode, the average output power level is higher than that

of mode B, but lower than the power level that results in the out-of-band emissions improvement caused by the addition of the PPR block to be lost. Therefore, both average output power and the out-of-band emissions performance are improved 5 compared to the transmitter implemented without the PPR block while there is an acceptable level of in-band waveform quality degradation.

Within mode D, the average output power for the power amplifier is maximized, while the out-of-band emissions 10 and in-band waveform quality reach their respective worst acceptable limits. In this mode, the configurable threshold signal T and the power amplifier drive level are optimized such that together, the out-of-band emissions reaches its maximum acceptable limit and the in-band waveform quality 15 reaches its minimum acceptable limit, with neither failing. This results in the transmitter implemented with the PPR block reaching the maximum allowable average output power.

Although these four modes are described, one skilled in the art could contemplate other setups for a 20 transmitter with the PPR block of the present invention. The main consideration is the trade off between out-of-band emissions, in-band waveform quality, and average output power.

Persons skilled in the art will appreciate that 25 there are alternative implementations and modifications possible to use an apparatus similar to that described above to reduce peak power periods within data signals, and that the above implementation is only an illustration of this embodiment of the invention. The scope of the invention, 30 therefore, is only to be limited by the claims appended hereto.